STIC EIC 2100 117723
Search Request Form 126

Today's Date: 25 March 2004

What date would you like to use to limit the search?
Priority Date: 23 Dec 1997 Other:

Name Thomas Seal
AU 2135 Examiner # 76980
Room # 4D11 Phone 308-4552
Serial # 09/755 0511

Format for Search Results (Circle One):
PAPER DISK EMAIL

Where have you searched so far?
USP DWPI EPO JPO ACM IBM TDB
IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES NO
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Split key

$d = d_1 + d_2$

d_1 = most significant portion (bits)

d_2 = Least Significant portion LSB

Encrypt

$E(d_2)$

and store with d_1:

$d_1 \,||\, E(d_2)$

STIC Searcher Geoffrey St. Leger Phone 308-7800
Date picked up 3/25/04 Date Completed 3/25/04

File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200419
(c) 2004 Thomson Derwent

Set	Items	Description
S1	5810	(LEAST OR LESS OR LESSER OR SMALLEST OR SMALLER OR LOW???)-(1W)SIGNIFICAN??
S2	5915	(MOST OR GREATEST OR LARGEST OR HIGH???)(1W)SIGNIFICAN??
S3	87	S1(10N)S2(10N)(SPLIT???? OR DIVID??? OR BREAK??? OR BROKEN OR SEPARATE? ? OR SEPARATION OR CHOP???? OR CARV???)
S4	1007	S1(10N)S2
S5	6	S4(5N)(NUMBER? ? OR NUMERAL? ?)(5N)(SPLIT???? OR DIVID??? - OR BREAK??? OR BROKEN OR SEPARATE? ? OR SEPARATION OR CHOP???? OR CARV???)
S6	13560	(LOW??? OR SMALLEST)(1W)ORDER
S7	27943	(HIGH??? OR LARGEST)(1W)ORDER
S8	4790	S6(10N)S7
S9	37	S8(5N)(NUMBER? ? OR NUMERAL? ?)(5N)(SPLIT???? OR DIVID??? - OR BREAK??? OR BROKEN OR SEPARATE? ? OR SEPARATION OR CHOP???? OR CARV???)

5/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06464044 **Image available**
2-CHANNEL HVQ COMPRESSION METHOD

PUB. NO.: 2000-049619 [JP 2000049619 A]
PUBLISHED: February 18, 2000 (20000218)
INVENTOR(s): NGUYEN UOC H
NGUYEN KIEN T
CLAPROTH ABRAHAM E
KANG SANG-CHUL
LEE CHIA-HAO
APPLICANT(s): XEROX CORP
APPL. NO.: 11-180854 [JP 99180854]
FILED: June 25, 1999 (19990625)
PRIORITY: 106581 [US 98106581], US (United States of America), June 29, 1998 (19980629)
INTL CLASS: H03M-007/30; H04N-001/41; H04N-007/24

ABSTRACT

PROBLEM TO BE SOLVED: To optimize compression efficiency by dividing a word into a high- order bit and a low-order bit, compressing them in respectively suitable different procedures and then combining and re-connecting them.

SOLUTION: For a gray zone byte map 16, a code word generated in a hierarchical vector quantizer HVQ encoder 10 is compressed in an LZ encoder 11 and sent to a decoder and a byte map version is generated in an HVQ decoder 12 and inputted to a quantizer 14. In the quantizer 14, it is **divided** into the respectively prescribed **numbers** of **most significant** bits MBS and **least significant** bits LBS, the MBS is compressed by O or small compressibility and the LBS is compressed by large compressibility separately by the encoder, then they are added, sent to the decoder parallelly to the original code word which is the output of the encoder 11 and re-connected with the original code word and video signals are obtained. By enlarging the compressibility of the LBS of low importance in such a manner, the compression efficiency is improved without damaging image quality.

5/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015963459 **Image available**
WPI Acc No: 2004-121300/200412
XPIX Acc No: N04-097156

Logarithm computation apparatus for floating point number, multiplies exponent in floating point number with logarithm of its base, and adds it logarithm of most signification bit in mantissa of the number

Patent Assignee: SILICON INTEGRATED SYSTEMS CORP (SILI-N)
Inventor: LU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040010532	A1	20040115	US 2002191214	A	20020709	200412	B

Priority Applications (No Type Date): US 2002191214 A 20020709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040010532	A1		11	G06F-007/38	

Abstract (Basic): US 20040010532 A1
NOVELTY - A multiplier (210) multiplies the exponent in a floating

point number with logarithm of its base. The multiplication result is added with the logarithm of **most significant** bit (Ax) in the mantissa of the **number** . The **least significant** bit (Bx) of the mantissa, is **divided** by a specific value and is approximated by a Taylor-series approximation unit (250).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for logarithm computation method.

USE - For computing logarithm for base of floating point number in computer system.

ADVANTAGE - Precisely and efficiently computes logarithm to the base of both the large and small floating point numbers.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the logarithm computation apparatus.

logarithm computation apparatus (200)
multiplier (210)
adders (230,260)
divider (240)
Taylor-series approximation unit (250)
pp; 11 DwgNo 3/5

Title Terms: LOGARITHM; COMPUTATION; APPARATUS; FLOAT; POINT; NUMBER; MULTIPLICATION; EXPONENT; FLOAT; POINT; NUMBER; LOGARITHM; BASE; ADD; LOGARITHM; BIT; MANTISSA; NUMBER
Derwent Class: T01
International Patent Class (Main): G06F-007/38
File Segment: EPI

5/5/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

012927687 **Image available**
WPI Acc No: 2000-099523/200009
XRPX Acc No: N00-076868

Unequal compression of MSBs and LSBs using Hierarchical Vector Quantization (HVQ) e.g. for transmission or storage of computer data

Patent Assignee: XEROX CORP (XERO)
Inventor: CLAPROTH A E; KANG S; LEE C; NGUYEN K T; NGUYEN U H
Number of Countries: 027 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 969670	A1	20000105	EP 99304634	A	19990615	200009	B
JP 2000049619	A	20000218	JP 99180854	A	19990625	200020	
US 6205252	B1	20010320	US 98106581	A	19980629	200118	
EP 969670	B1	20030219	EP 99304634	A	19990615	200314	
DE 69905428	E	20030327	DE 605428	A	19990615	200329	
			EP 99304634	A	19990615		

Priority Applications (No Type Date): US 98106581 A 19980629
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 969670	A1	E	13	H04N-007/28	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000049619	A		6	H03M-007/30	
US 6205252	B1			G06K-009/36	
EP 969670	B1	E		H04N-007/28	
Designated States (Regional): DE FR GB					
DE 69905428	E			H04N-007/28	Based on patent EP 969670

Abstract (Basic): EP 969670 A1

NOVELTY - A process of compressing an original word having a **number** of bits comprises **splitting** the word into the **most significant** bits and the **least significant** bits (32,33). Compressing the **least significant** bits in a first compressor (35), compressing the **most significant** bits in a second compressor (34), and outputting an output word comprising the combination of the result of the two compressing steps.

USE - For transmission or storage of computer data.
ADVANTAGE - Different amount of compression can be applied to each portion of word, hence yielding either less loss or greater compression, compared to the original method. Improves the system performance of a compressor using HVQ.
DESCRIPTION OF DRAWING(S) - The diagram shows a one-channel arrangement for coding a pixel split into its most and least significant bits.
most and least significant bits (32,33)
compressors. (34,35)
pp; 13 DwgNo 3/9
Title Terms: UNEQUAL; COMPRESS; HIERARCHY; VECTOR; QUANTUM; TRANSMISSION; STORAGE; COMPUTER; DATA
Derwent Class: T01; T03; U21; W01
International Patent Class (Main): G06K-009/36; H03M-007/30; H04N-007/28
International Patent Class (Additional): G06K-009/46; G06T-009/00; H04N-001/41; H04N-007/24; H04N-007/36
File Segment: EPI

5/5/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

[illegible] **Image available**
WPI Acc No: 1999-253295/199921
XRPX Acc No: N99-188481
Incrementor for microprocessor
Patent Assignee: INTEL CORP (ITLC)
Inventor: JOSHI V; KUMAR S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5889693	A	19990330	US 97851220	A	19970505	199921	B

Priority Applications (No Type Date): US 97851220 A 19970505
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5889693	A		18	G06K-007/50	

Abstract (Basic): US 5889693 A
NOVELTY - An extraction unit (440) **separates** the binary **number** into **least significant** bits and **most significant** bits. The **least significant** bits are adjusted if the increment is three. The **most significant** bits are incremented and combined with **least significant** bits.
USE - For microprocessor.
ADVANTAGE - Faster operation than ripple carry is achieved using less area and few components. Overall logic size is reduced by using less number of logic blocks.
DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of [illegible]
extraction unit (440)
pp; 18 DwgNo 4/6
Title Terms: MICROPROCESSOR
Derwent Class: T01
International Patent Class (Main): G06K-007/50
File Segment: EPI

5/5/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

008742949 **Image available**
WPI Acc No: 1991-246965/199134
XRPX Acc No: N91-188307
Fast response digital appts. for interfacing sensors to systems -

converts integer number into variable duty cycle pulse train of predetermined repetition rate

Patent Assignee: BORG WARNER AUTOMOTIVE INC (BORW)
Inventor: LANDMANN W S
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 442209	A	19910821	EP 90313524	A	19901212	199134	B
US 5053769	A	19911001	US 90478287	A	19900212	199142	
CA 2031881	A	19910813				199143	
JP 4297142	A	19921021	JP 912190	A	19910111	199249	

Priority Applications (No Type Date): US 90478287 A 19900212
Cited Patents: GB 2196498; US 4685114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 442209	A				
Designated States (Regional): DE ES GB					
JP 4297142	A		16	H04B-014/02	

Abstract (Basic): EP 442209 A

The derived integer **number** indicative of the sensor position is **divided** into a **most significant** part and a **least significant** part. The **most significant** part is converted into a sequence of predetermined **number** of pulses in which the duty cycle of each pulse represents a value which corresponds to the most significant part. The least significant part is used to selectively alter the width of selected ones of the pulses.

The sequence of altered pulses may be integrated over the sequence or averaged to extract an analog output indicative of the original integer number.

USE/ADVANTAGE -For vehicle non-contact displacement sensor. High resolution using higher frequency pulse train. Fast response. May be implemented in hardware or software. (10pp Dwg.No.1/11

Title Terms: FAST; RESPOND; DIGITAL; APPARATUS; INTERFACE; SENSE; SYSTEM; CONVERT; INTEGER; NUMBER; VARIABLE; DUTY; CYCLE; PULSE; TRAIN; PREDETERMINED; REPEAT; RATE
Index Terms/Additional Words: VEHICLE
Derwent Class: S02; U22; X22
International Patent Class (Main): H04B-014/02
International Patent Class (Additional): G01D-021/00; H03K-007/08; H03M-001/66; H03M-005/08
File Segment: EPI

5/5/6 **(Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

008720396 **Image available**
WPI Acc No: 1991-224413/199131
XRPX Acc No: N91-171291

Exponent difference determination method - using comparator to determine which exponent is higher, while multiplexer selects required exponent difference

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: DREHMEL R A; HILKERF S A; HILKER S A
Number of Countries: 004 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 438962	A	19910731	EP 90480228	A	19901228	199131	B
US 5117384	A	19920526	US 90469628	A	19900124	199224	
			US 91702341	A	19910403		
EP 438962	A3	19920318	EP 90480228	A	19901228	199326	

Priority Applications (No Type Date): US 90469628 A 19900124; US 91702341 A 19910403
Cited Patents: NoSR.Pub; 2.Jnl.Ref; EP 296071; JP 63157231; US 2949231; US

[illegible]; US 4310879

[illegible] Details:

[illegible] No	Kind	Lan	Pg	Main IPC	Filing Notes
[illegible]962	A				
Designated States (Regional): DE FR GB					
US 5117384	A		12	G06F-007/38	Cont of application US 90469628

Abstract (Basic): EP 438962 A

The difference determination method uses an adder circuit (50) which determines which of exponents (A,B) are the larger and by how many bits a corresp. fraction portion of a floating point number must be shifted to make both exponents identical. Exponents (A,B) are split into two portions (52,54, and 56,58). Adder circuits (60,62,69) and compare circuit (66) are only as wide as the number of bits in the portion.

A comparator circuit (66) determines which exponent (A,B) is the higher, if either, while multiplexer (74) accordingly selects the required exponent difference. If the exponent difference indicates a shift of more bits than that of the fractional portion then the arithmetic operation is not necessary.

ADVANTAGE - Reduced adder width and increased speed. (14pp Dwg.No. 3/4)

Title Terms: EXPONENT; DIFFER; DETERMINE; METHOD; COMPARATOR; DETERMINE; EXPONENT; HIGH; MULTIPLEX; SELECT; REQUIRE; EXPONENT; DIFFER

Derwent Class: T01

International Patent Class (Main): G06F-007/38

International Patent Class (Additional): G06F-007/50

[illegible]ument: EPT